Wed, 19 Jul 2006, 2:16:04 PM EST

Edit an existing query or compose a new query in the Search Query Display.

Select a search number (#) to:

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- Combine search queries using AND, OR, or NOT
- Delete a search
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Search Query Display

Recent Search Queries

#1	((memory and (bank* or module* or segment*))<in>metadata)
#2	(simultaneous and access<IN>metadata)
#3	(multiplexor or multiplexer<IN>metadata)
#4	(synchronous* and access<IN>metadata)
#5	(shared memory<IN>metadata)
#6	(rotating and selector*<IN>metadata)
#7	((single or uni or one) and bit<IN>metadata)
#8	(ratcheting and distributor*<IN>metadata)
#9	(((memory and (bank* or module* or segment*))<in>metadata)) <AND> ((simultaneous and access<IN>metadata))
#10	((((memory and (bank* or module* or segment*))<in>metadata)) <AND> ((simultaneous and access<IN>metadata))) <AND> ((multiplexor or multiplexer<IN>metadata))
#11	(((((memory and (bank* or module* or segment*))<in>metadata)) <AND> ((simultaneous and access<IN>metadata))) <AND> ((multiplexor or multiplexer<IN>metadata))) <AND> ((synchronous* and access<IN>metadata))
#12	((((((memory and (bank* or module* or segment*))<in>metadata)) <AND> ((simultaneous and access<IN>metadata))) <AND> ((multiplexor or multiplexer<IN>metadata))) <AND> ((synchronous* and access<IN>metadata))) <AND> ((rotating and selector*<IN>metadata))

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	253	370/395.7.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 14:01
L2	2168	370/412.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 14:01
L3	24383536	@ad<"20030717"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 14:03
L4	98	(Whay near Lee).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 14:03
L5	0	(Chong near "JR.").in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 14:03
L6	16	(walter near Nixon).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 14:03
L7	29965	"711"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 14:03
L8	46278	memory adj (bank$2 or module$2 or segment$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 14:03
L9	368054	multiplex$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 14:03

EAST Search History

L10	1	ratcheting adj distributor$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 14:03
L11	1929	rotat$4 adj selector$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 14:03
L12	2249021	switch$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 14:03
L13	2136089	synchronous$4 or simultaneous$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 14:03
L14	20907	shared adj memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 14:03
L15	234	successive adj clock adj cycle	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 14:05
L16	308	((single or uni or one) adj bit) same rotat$4 same clock$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 14:06
L17	111	4 or 6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 14:06
L18	11978	8 and 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 14:06
L19	7606	18 and 12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 14:07

EAST Search History

L20	4	19 and 11	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 14:07
L21	3	20 and 13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 14:07
L22	0	21 and 14	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 14:08
L23	0	21 and 15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 14:08
L24	1	21 and 16	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/19 14:08

Terms used
memory bank synchronous access simultaneous operation single bit operation multiplexor

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Relevance scale

1 Preprocessors in a data communication computer environment

David L. Mills

October 1969 **Proceedings of the first ACM symposium on Problems in the optimization of data communications systems**

Publisher: ACM Press

Full text available: pdf(1.26 MB) Additional Information: full citation, abstract, references, index terms

Realizing the need for a highly adaptable transmission control unit to interface varied terminal equipment to the Michigan Timesharing System (MTS), the University of Michigan initiated in 1965 the development of a special control unit to be used in conjunction with the System/360 Model 67. Called the Data Concentrator The design approach taken in the Data Concentrator has been to nucleate about a small general-purpose computer a number of special-purpose interfaces to the variou ...

2 A parallel bit map processor architecture for DA algorithms

Tom Blank, Mark Stefik, Willem vanCleemput

June 1981 **Proceedings of the 18th conference on Design automation**

Publisher: IEEE Press

Full text available: pdf(748.21 KB) Additional Information: full citation, abstract, references, citings, index terms

Bit maps have been used in many Design Automation (DA) algorithms such as printed circuit board (PCB) layout and integrated circuit (IC) design rule checking (DRC). The attraction of bit maps is that they provide a direct representation of two-dimensional images. The difficulty with large scale use of bit maps (e.g., for DRC on VLSI) is that the large amounts of data can consume impractical amounts of computation on sequential machines. This paper describes a processing architect ...

3 Prototyping time- and space-efficient computations of algebraic operations over dynamically reconfigurable systems modeled by rewriting-logic

M. Ayala-Rincón, C. H. Llanos, R. P. Jacobi, R. W. Hartenstein

April 2006 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 11 Issue 2

Publisher: ACM Press

Full text available: pdf(838.46 KB) Additional Information: full citation, abstract, references, index terms

Many algebraic operations can be efficiently implemented as pipe networks in arrays of functional units such as systolic arrays that provide a large amount of parallelism.

However, the applicability of classical systolic arrays is restricted to problems with strictly regular data dependencies yielding only arrays with uniform linear pipes. This limitation can be circumvented by using reconfigurable systolic arrays or reconfigurable data path arrays, where the node interconnections and operations ...

Keywords: Fast Fourier Transform (FFT), Term Rewriting Systems (TRS), algebraic manipulation, dynamically reconfigurable systems, reconfigurable computing, rewriting-logic, systolic arrays

4 Performance of the vectorial processor VEC-SM2 using serial multiport memory

J. Jorda, A. Mzoughi, O. Lafontaine, D. Litaize

January 1996 **Proceedings of the 10th international conference on Supercomputing**

Publisher: ACM Press

Full text available: pdf(777.69 KB) Additional Information: full citation, references, index terms

5 Plasma: an FPGA for million gate systems

R. Amerson, R. Carter, W. Culbertson, P. Kuekes, G. Snider, Lyle Albertson

February 1996 **Proceedings of the 1996 ACM fourth international symposium on Field-programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(264.25 KB) Additional Information: full citation, references, citings, index terms

Keywords: FPGA, custom computing, register files

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